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Electrochemical Anodization of Silicon-on-Insulator Wafers Using an AC

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Electrochemical anodization of bulk silicon has applications in many micromachining processes. However, its use for silicon photonics is limited because silicon-on-insulator (SOI) wafers cannot be anodized using a conventional process because of the buried oxide. We overcome this using an alternating potential to induce an ac across an SOI wafer, treating it as a capacitative structure. The resultant surface roughness is comparable to that obtained using conventional anodization, and uniform etching across a 6 mm exposed surface is obtained with a minimum patterned linewidth of 2.5 μm in the device layer.
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Silicon-on-insulator (SOI) based photonic components utilize both the low refractive index and near atomic smoothness of the buried oxide to provide a low loss optical confinement layer. Fabrication of many different types of photonic devices in silicon-based and SOI materials has been intensively researched,[1-4] with most approaches combining some form of lithography for patterning and etching to remove the surrounding material. Each process step introduces additional roughness,[5-7] resulting in high propagation losses in SOI waveguides, though subsequent oxidation greatly helps to reduce the roughness.[8,9] For example, in Ref. 10 and 11, the propagation loss for single-mode SOI waveguides was reduced from 32 to 0.8 dB/cm when the sidewall roughness was reduced from 10 to 2 nm.

Electrochemical anodization of bulk silicon[12] gives a low surface roughness, typically 2 nm for anodized layer thicknesses of a few hundred nanometers.[13] A microfabrication process based on mega-electron-volt ion irradiation in conjunction with electrochemical anodization of bulk silicon was recently developed for micromachining a variety of surface-relief patterns and variable wavelength and intensity photoluminescence.[14-17] A beam of mega-electron-volt protons or helium ions irradiates the p-type wafer surface. As ions penetrate the silicon, they create lattice damage in the form of vacancy–interstitial pairs. The irradiated material is more resistive than the surrounding unirradiated areas,[18] so a lower hole current and hence a lower local etching rate occur during subsequent electrochemical anodization, producing either a surface-relief pattern or completely undercut structures suitable for waveguide formation. Irradiation through a thick, patterned photoresist[19] was used to produce silicon-on-oxidized-porous-silicon strip waveguides in bulk, p-type wafers with widths and heights from 1.5 to 3.0 μm. After high temperature annealing to remove the lattice damage and for oxidation smoothening, propagation losses of ~1 dB/cm were obtained.[20]

This process would be ideal for fabricating low loss SOI photonic components. However, conventional dc electrochemical anodization relies on a constant current flowing to the front surface of bulk silicon, and the oxide layer in SOI prevents the flow of a continuous current. Alternative approaches to anodizing SOI have been studied, such as lateral anodization across the front surface or stain etching,[12] but none produce a high uniformity or low roughness. This study shows how this limitation can be overcome using an induced ac to anodize SOI wafers. Consider an SOI wafer as a simple parallel plate capacitor, with the substrate and device silicon layers forming the conducting plates, separated by the buried silicon dioxide dielectric. An alternating potential applied across the wafer induces an ac across the dielectric, which results in anodization of the device layer surface for half of the alternating cycle in which the hole current flows in this direction, with hydrogen evolved on the surface during the second half of the cycle. Both wafer surfaces are anodized, though anodization of the back surface may be stopped by replacing the HF electrolyte in this half of the cell with a nonanodizing solution. This approach is used to uniformly anodize SOI wafers with a surface roughness comparable to that obtained using conventional dc anodization.

For a given root-mean-square (rms) current measured during ac anodization, one therefore expects the etch rate to be half that for dc anodization because both surfaces are etched. This agrees with Ref. 21, where it was shown that ac and dc anodization of unpatterned bulk silicon resulted in similar photoluminescence and surface roughness for the same total charge transfer.

Figure 1a shows patterning of the SOI device layer using ion irradiation through a 10 μm thick poly(methyl methacrylate) (PMMA) photoresist. A fluence of $1 \times 10^{15}/\text{cm}^2$ at 500 keV protons was used, with a range of 7.7/6.1 μm in PMMA/Si, so only the exposed wafer areas were irradiated. After the removal of the PMMA layer, a double-sided cell was used for ac anodization (Fig. 1b), with both surfaces exposed to the electrolyte [HF (48%): water:ethanol in the ratio of 1:1:2] over a wafer area of 1.2 × 1.2 cm. A 50 Hz mains-coupled variable ac voltage supply was used with a 30 Ω series resistor to limit the induced current. The irradiated areas of the device layer remain unanodized because the high ion fluence renders them highly resistive, so all the hole current flows to adjacent unirradiated areas, which are progressively anodized with time. The porous silicon was then removed with potassium hydroxide, leaving a patterned SOI device layer (Fig. 1c).

In ac anodization of SOI wafers, the induced current flow across the buried oxide may change significantly for a given ac potential, so the quoted values of rms anodization current are the average values over the full anodization period, while using the variable voltage ac supply to maintain an ac current as constant as possible. A further complication to defining the ac anodization current density is that the effect of patterned ion irradiation is to deliberately limit anodization to only certain parts of the exposed surface, typically half of the exposed surface in this case. This is further complicated by the greater etch rate/depth observed at the exposed wafer edges (shown later in Fig. 4) as a result of a greater etch current at the edges compared to the center. Values of etch current and etch current density given here are to be interpreted in light of the above.

We first compared the effects of ac and dc anodization using this cell with 2 × 2 cm pieces of 10 Ω cm p-type bulk silicon. Patterned surfaces were produced by irradiating through a thick resist patterned with 20 and 10 μm wide lines and gaps. One sample was anodized in ac mode to a depth of 250 nm using an rms current density of 50 mA/cm^2 for a period of 30 s, and another sample anodized in dc mode to the same depth using a current density of 50 mA/cm^2 for a period of 15 s. After the removal of the porous silicon, the surfaces were measured with an atomic force microscope

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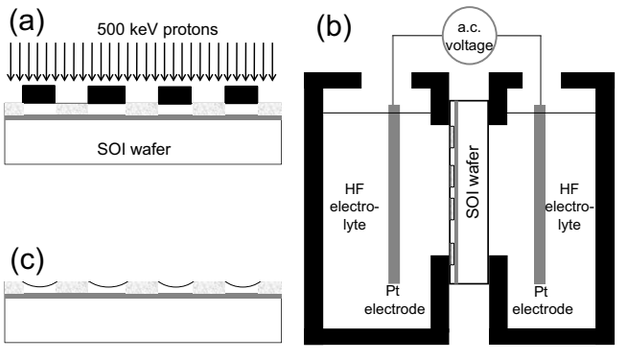

Figure 1. Schematic of the ac anodization process. (a) Proton irradiation through a thick patterned PMMA layer (shown in black) results in a patterned SOI device layer. (b) Teflon cell (shown in black) for ac anodization of SOI wafer. (c) Removal of porous silicon producing a patterned SOI device layer.

(AFM). The height profiles, recorded perpendicular to the etched lines in Fig. 2, are very similar. The anodized surfaces at the unirradiated regions are convex because deflection of the hole current away from the irradiated regions usually produces a higher anodization rate at the boundary with adjacent unirradiated regions.[18] The width of the boundaries between the irradiated lines and the anodized regions is about 2 μm. The roughness measured from 3 × 3 μm regions at the top irradiated surfaces is 0.30 nm for modes, as one would expect because it is effectively a virgin surface. The roughness values of the anodized surfaces are 0.8 and 0.7 nm in ac and dc modes, respectively, with an error of ±0.25 nm. This behavior agrees well with Ref. 21 and demonstrates that ac anodization produces similar patterned features from ion irradiated areas as does dc anodization.

An SOI wafer (ULTRASIL) with a 10 Ω cm p-type device layer thickness of 10 μm and a buried oxide thickness of 1 μm was similarly patterned with a fluence of $1 \times 10^{15}/\text{cm}^2$ and then ac anodized to a depth of 5 μm over a 6 min period. An alternating voltage of 50–100 V was used to induce an rms ac current of 60 mA, equivalent to a wafer impedance of ~2 kΩ. Figure 3 shows cross-section scanning electron micrographs (SEMs) of the central portion of the anodized wafer. The gaps between the irradiated lines were all anodized to the same depth (Fig. 3a), demonstrating that the anodization rate was uniform across this central portion of the anodized surface. In Fig. 3b, the anodized surfaces have a concave profile, compared with the convex profiles in Fig. 2. Such concave profiles are associated with heavily irradiated, closely spaced features in

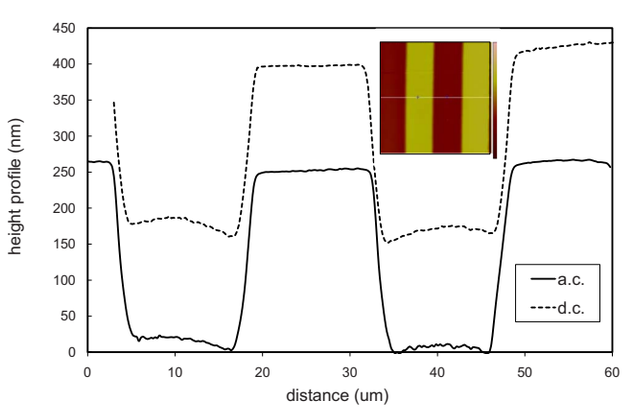

Figure 2. (Color online) AFM line profiles 10 Ω cm p-type bulk silicon anodized in ac and dc modes, offset for clarity. The inset shows a 60 × 60 μm AFM image of the ac anodized wafer surface.

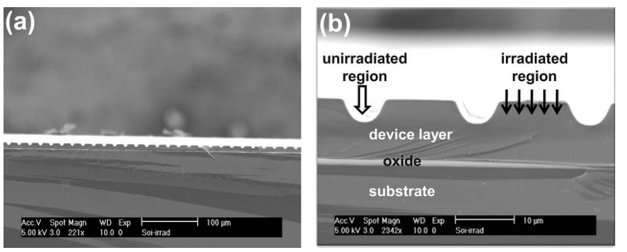

Figure 3. Cross-section SEMs of the central portion of the ac anodized SOI wafer at different magnifications.

highly resistive wafers[18] where the current deflected from the opposing irradiated regions creates a maximum at the central point between them, producing in a more deeply etched, concave surface.

Further study confirmed that ac anodization produced uniform features across the central 6 mm width of the exposed 12 mm wide SOI surface. However, toward the cell boundary, the anodization rate varies laterally, resulting in a nonuniform depth of the gaps between the etched lines (Fig. 4a). Furthermore, at the cell boundary, a deep groove tends to form (Fig. 4b). Because anodization occurs at a much faster rate here, care is needed during anodization. Once the buried oxide layer at the groove is exposed, the HF electrolyte rapidly dissolves it and creates a much lower resistivity conducting path to the surface, effectively short-circuiting the wafer. The current flowing must therefore be carefully monitored, and the current flow stopped when it rapidly increases. AC anodization of SOI wafers exhibits similar problems as does dc anodization of bulk, high resistivity wafers[22] where similar problems of groove formation and lateral nonuniformities in the anodization rate are observed.

In Fig. 1, the thick photoresist layer required to stop 500 keV protons limits the minimum lateral size of the irradiated areas to about 5 μm. We developed a maskless process for high energy ion irradiation with the beam focused to a long line, up to 6 mm in length, with a width of about 1 μm. This was done by exciting the quadrupole lenses of a nuclear microprobe focusing system[23] in a particular manner so that the beam was focused in one plane but highly defocused in the orthogonal plane. This is suitable for waveguide formation of SOI without the commonly encountered problems of proton beam writing using a beam focused to a point, namely beam fluctuations from one position to another. The AFM image in Fig. 5 shows such a line irradiated in the same SOI wafer material, with a fluence of $5 \times 10^{14}/\text{cm}^2$ of 2 MeV protons. After ac anodizing the SOI device layer to a depth of 2 μm using an induced rms ac current of 50 mA, the linewidth is 2.5 μm, the best value achieved to date.

In summary, we have shown how electrochemical anodization of SOI wafers can be achieved using an induced ac across the buried oxide, with a roughness comparable to that obtained using conventional anodization. This opens up a route to fabricating SOI-based

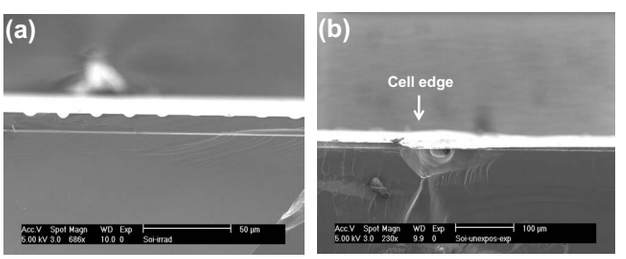

Figure 4. Cross-section SEMs of the ac anodized SOI wafer close to the cell edge. (a) The nonuniform lateral anodization. (b) The deep groove forming at the cell edge.

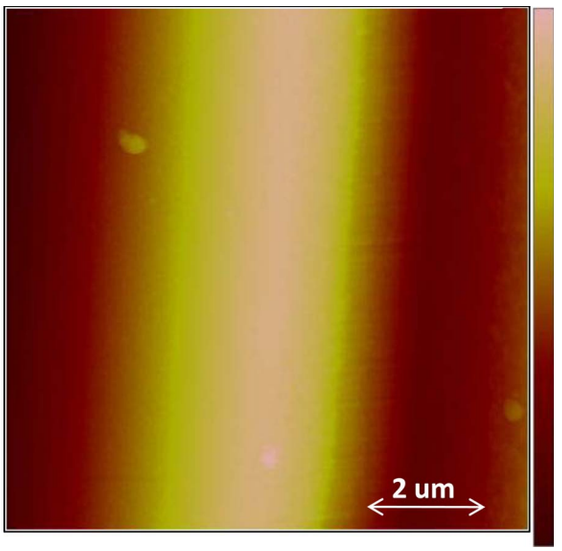

Figure 5. (Color online) AFM image of a single irradiated line in SOI after ac anodization using a line focus of 2 MeV protons.

photonic components based on electrochemical anodization, and we are investigating the use of thinner device layers to reduce the minimum achievable linewidth from its present value of 2.5 μm.

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