

Effects of oxide formation around core circumference of silicon-on-oxidized-porous-silicon strip waveguides

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Received August 7, 2009; revised September 9, 2009; accepted September 10, 2009;
posted September 17, 2009 (Doc. ID 115435); published October 8, 2009

We have studied the effect of oxidation on the propagation loss and surface roughness of silicon-on-oxidized-porous-silicon strip waveguides fabricated using proton-beam irradiation and electrochemical etching. A thin thermal oxide is formed around the core of the waveguide, enabling the symmetric reduction of core size and roughness on all sides. Significant loss reduction from about 10 dB/cm to 1 dB/cm has been obtained in TE and TM polarizations after oxidation smoothening of both the bottom and the sidewalls by 20 nm. This corresponds well with simulations using the beam-propagation method that show significant contributions from both surfaces. © 2009 Optical Society of America

OCIS codes: 230.7370, 220.4000, 290.5880.

Recently, there has been rapid progress in the development of a silicon photonics integrated circuit to meet the growing demand for faster interconnection and higher data bandwidth. Most conventional photonic devices are built on a silicon-on-insulator (SOI) substrate owing to its compatibility with microelectronics technologies and the high-index contrast between silicon and silicon dioxide [1]. This means that ultracompact optical devices with tight bends of a few micrometers can be densely packed and integrated with microelectronic circuits on a single chip.

Conventional SOI substrates are fabricated using separation by implanted oxygen (SIMOX) or the Smart-Cut process [2,3]. A lesser used technique for SOI fabrication is by full isolation by oxidized porous silicon (FIPOS), which was first developed by Imai *et al.* [4] for device isolation in microelectronics. The low cost and easy implementation of electrochemical etching has made it an attractive alternative to dry etching. Proton implantation converts *p*- to *n*-type silicon islands, which are selectively inhibited from porous silicon (PS) formation. Compared to SIMOX, this process gives more freedom in controlling the thickness of the overlying silicon layer owing to the well-defined ion range with energy and higher penetration depth of protons. This means that widely varying thickness of the silicon overlayer can be obtained. The oxide thickness can also be tuned easily with the etching time.

There has been much research on the optical properties of structures fabricated using SIMOX [5] and Smart Cut [6] but not FIPOS. Recently, we demonstrated the ability to fabricate high-index contrast silicon-on-oxidized porous-silicon (SOPS) waveguides with low loss directly in silicon without the need for an SOI substrate [7,8]. Here we aim to investigate the propagation loss mechanism of SOPS waveguide with oxidation. Owing to the high surface area/volume ratio, the oxidation rate of PS is orders of magnitude higher than Si. Oxidation produces a fully

oxidized PS layer and a thin thermal oxide around the waveguide core [2]. This enables surface roughness reduction on all sides of the waveguide, including the bottom interface. We have studied the effect of oxidation on surface roughness from the underside of the waveguide using atomic force microscopy (AFM), since these surfaces are most affected by the fabrication process. Scattering loss due to bottom and sidewall roughness are then simulated using the beam-propagation method and compared with experimental loss data measured at a wavelength of 1550 nm.

Figure 1 shows a schematic diagram of the waveguide fabrication process carried out on bulk *p*-type silicon (0.7 Ω cm) using 250 keV protons. Previously, we have employed a highly focused beam of protons with ~200 nm spatial resolution to pattern waveguide structures. Although the direct-write approach is useful for rapid prototyping, it has a low throughput owing to the low currents of picoamperes within the focused beam. In this work, a broad uniform proton beam of several hundreds of nanoamperes have been delivered onto a lithographically patterned silicon over a large area of 3 × 3 cm [Fig. 1(a)] [10]. This process allows rapid mass production of waveguides and also eliminates any surface roughness caused by stage scanning and beam intensity fluctuations in

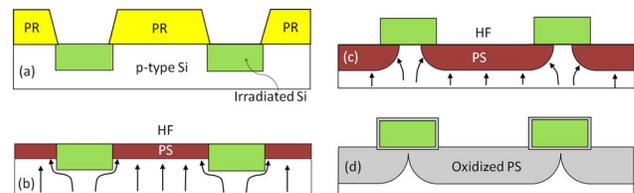


Fig. 1. (Color online) (a) Proton-beam irradiation through a photoresist (PR) mask and (b) PS formation until the end of ion range. The arrows show the holes bending around the irradiated regions during etching [9]. (c) Subsequent PS removal and etching to isolate the structures; (d) a two-step oxidation process.

the direct-writing approach. Details of the etching conditions and the optical characterization setup can be found in [8].

Figure 2(a) shows an array of $5.2 \times 2.6 \mu\text{m}$ waveguides written with a fluence of $5 \times 10^{13}/\text{cm}^2$. The cross-sectional scanning electron microscopy (SEM) image in Fig. 2(b) reveals a rectangular Si core that is optically confined with PS cladding. Owing to the isotropic etching process, a cusp is formed at the point where the waveguide is detached from the Si substrate. As the etching is not completely stopped in the irradiated region, a thin layer of PS can still be seen around the waveguide [Fig. 2(c)]. After a two-step oxidation process in air ambient at 300°C for 3 h and 1000°C for 6 h [Fig. 2(d)], the PS cladding layer becomes fully oxidized, while the core is being consumed from the PS/Si interface. A thin layer of thermal oxide ~ 350 nm is produced around the core, reducing the width and height to $4.5 \mu\text{m}$ and $1.9 \mu\text{m}$, respectively, as well as the cusp size. The refractive index of PS and oxidized PS is found to be 1.68 and 1.36, respectively, from fitting the reflectance spectra using the Bruggeman formula [11]. From the inset in Figs. 2(c) and 2(d), the output light observed at the end facet of the oxidized waveguide is much brighter than that of the unoxidized waveguide.

Optical characterization of the waveguides is carried out for both TE and TM polarizations at a wavelength of 1550 nm. Figure 3 shows the cutback technique used to characterize the propagation loss of the waveguides, whereby the output power from the waveguides is determined for various lengths. Before oxidation, the waveguide shows a high loss of 10.3 ± 0.6 dB/cm and 9.1 ± 0.3 dB/cm in the TE and TM polarizations. This is reduced significantly to 1.6 ± 0.1 dB/cm and 1.4 ± 0.2 dB/cm, respectively, after oxidation.

Understanding the mechanism that limits the optical losses is important to improve the quality of the waveguides. For the resistivity of silicon used in our

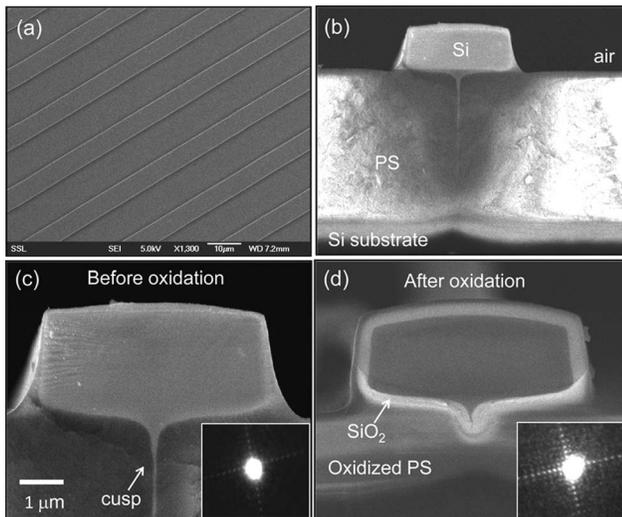


Fig. 2. SEM image of the (a) top and (b) cross sectional and close-up views of the waveguides (c) before and (d) after oxidation. Inset, the respective output light imaged from each facet.

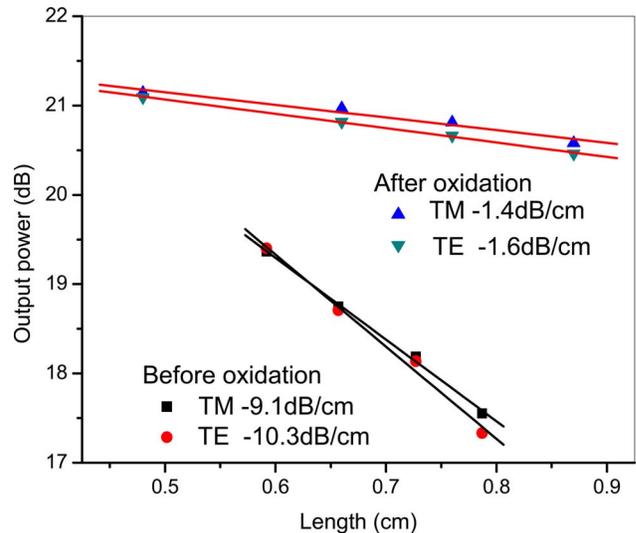


Fig. 3. (Color online) Cutback measurements of waveguide before and after oxidation.

experiment, the absorption due to free carriers is about 0.5 dB/cm. Surface roughness is a significant source of loss for such a high-index-contrast waveguide, since the scattering loss scales proportionally to $\Delta n^2 = (n_{\text{core}}^2 - n_{\text{clad}}^2)$ [12]. Conventional SIMOX processing produces waveguides with atomically smooth top and bottom surfaces after high-temperature annealing of the implanted oxide layer. Therefore the major contribution to the propagation loss is from the sidewall roughness introduced by the lithographic process [13]. For the FIPOS process, interface roughness is formed at the PS/Si dissolution front owing to the lithographic roughness and the etching process [14]. Both the sidewalls and the bottom surfaces are affected and need to be determined. This is done by removing the cladding layer so that direct measurement of the underside of the waveguide can be taken using AFM. The PS cladding is removed using a diluted KOH solution and the oxidized PS using diluted HF solution. Since the top surface is only mildly affected by etching process, it retains a smooth surface roughness of approximately 2–3 nm, as shown from AFM measurement. In this case, its effect can be ignored.

Figure 4(a) shows the SEM picture of the underside of the waveguide with the cusp running along its length. The AFM images in Fig. 4(b) are taken over the bottom and sidewalls indicated by the white box. The results are displayed in Table 1. Oxidation reduces the sidewalls roughness from an rms roughness, σ , of 25 nm to 6 nm, and the bottom surfaces from 30 nm to 10 nm. The bottom surface shows higher roughness than the sidewalls because of the different etching conditions used to create them. A high-current density of $100 \text{ mA}/\text{cm}^2$ and low HF concentration of 12% was used to produce smoother sidewalls [8]. The resultant PS becomes cracked and had been removed in this case. The second etching step to undercut the structure was etched with a current density of $40 \text{ mA}/\text{cm}^2$ at 24% HF, so as to preserve the PS layer needed to isolate the core, but this adversely produces a rougher bottom surface [14]. The

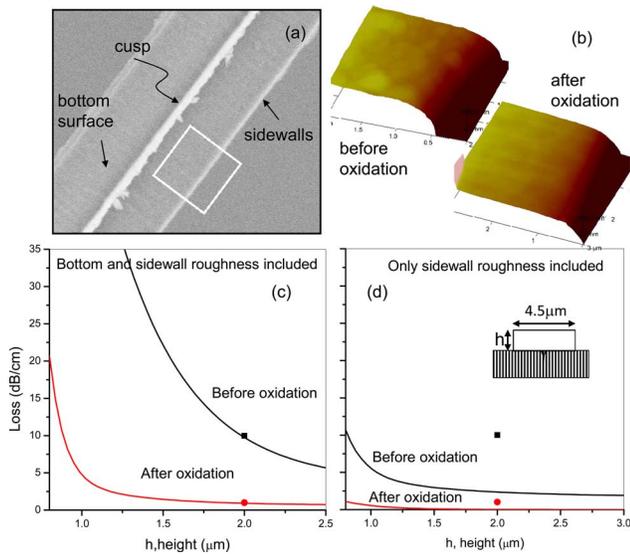


Fig. 4. (Color online) (a) SEM image and (b) AFM image of the underside of the waveguide. Calculated scattering loss (c) due to both the bottom and sidewalls and (d) due solely to sidewall roughness. The measured losses for waveguides (■) before and (●) after oxidation are overlaid on each plot.

autocorrelation length L_c is found to increase after oxidation for both the bottom surfaces and sidewalls. These are lower than previous L_c values of 190–270 nm reported on PS/Si interfaces [14]. Conventional SOI waveguides fabricated using a conventional lithography and etching process shows similar σ of about 10 nm but has lower L_c values of 50 nm [15].

Numerical simulations of the scattering loss were performed using 3D scalar BeamProp [16] with σ and L_c obtained from AFM measurements. BeamProp models the sidewall roughness using the physical mechanism developed by Marcuse *et al.* [17]. The bottom roughness profile taken from AFM measurements is included as a random perturbation to the height in the taper function. Simulations are based on the fundamental mode propagation, since the overlap integral analysis indicates that the fundamental mode carries most of the optical power in the regime where scattering loss is significant. A similar approach has been used previously by Lee *et al.* [13]. Figure 4(c) shows the simulated scattering loss from the bottom and sidewalls roughness as a function of height, for a constant width of 4.5 μm with a cusp included. The experimental data is in good agreement with the simulated data, indicating that surface roughness is the dominant contribution to propagation loss. When only the sidewall roughness is consid-

Table 1. Effect of Oxidation on Bottom and Sidewall Surfaces of the Waveguides

	Sidewalls		Bottom Surface	
	σ (nm)	L_c (nm)	σ (nm)	L_c (nm)
Before oxidation	25 ± 1	130 ± 10	30 ± 1	170 ± 10
After oxidation	6 ± 1	138 ± 12	10 ± 1	190 ± 12

ered [Fig. 4(d)], the measured loss is higher than the simulated data, indicating that bottom roughness contributes significantly to loss and has to be taken into account for accurate simulation. Previously, Lee *et al.* [13] showed that the loss increases rapidly with reducing width, owing to increased interaction of the mode with the sidewalls. In this case, the bottom surface roughness causes further increase in loss as the height reduces. These studies can be used to predict the loss of such waveguides as dimensions get smaller.

We have demonstrated large-scale production of SOPS waveguides with low losses after thermal oxidation using masked irradiation. Owing to the large differential oxidation rates of PS and Si, the 4- μm -thick PS cladding is fully oxidized, while a 350-nm-thin layer of thermal oxide is formed around the core. This reduces the width and height symmetrically by 700 nm and both the bottom and sidewalls roughness by about 20 nm. To obtain single-mode waveguides using this approach, a combination of high-resolution resist patterning using electron-beam lithography and shallower energy irradiation with ~ 50 keV protons is needed. Oxidation can further help shrink the core in a controlled manner within nanometer resolutions owing to the slow oxidation rate of 60 nm/h.

Funding from Lee Kuan Yew fellowship under Faculty of Research Council Startup Fund WBS R-144-000-230-112 and Singapore Ministry of Education Academic Research Fund Tier 2 under grant T207B1110 are acknowledged.

References

- G. T. Reed and A. P. Knights, in *Silicon Photonics: an Introduction* (Wiley, 2004).
- J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI* (Kluwer Academic, 1991).
- M. Bruel, *Electron. Lett.* **31**, 1201 (1995).
- K. Imai, *Solid-State Electron.* **24**, 150 (1981).
- B. N. Kurdi and D. G. Hall, *Opt. Lett.* **13**, 175 (1988).
- T. W. Ang, G. T. Reed, A. Vonsovici, A. G. R. Evans, P. R. Routley, and M. R. Josey, *Electron. Lett.* **35**, 977 (1999).
- E. J. Teo, A. A. Bettiol, M. B. H. Breese, P. Yang, G. Z. Mashanovich, W. R. Headley, G. T. Reed, and D. J. Blackwood, *Opt. Express* **16**, 573 (2008).
- E. J. Teo, A. A. Bettiol, P. Yang, M. B. H. Breese, B. Xiong, G. Z. Mashanovich, W. R. Headley, and G. T. Reed, *Opt. Lett.* **34**, 659 (2009).
- M. B. H. Breese, F. J. T. Champeaux, E. J. Teo, A. A. Bettiol, and D. Blackwood, *Phys. Rev. B* **73**, 035428 (2006).
- D. Mangaiyarkarasi, Y. S. Ow, M. B. H. Breese, L. S. Fuh, and X. Tang, *Opt. Express* **16**, 12757 (2008).
- D. E. Aspnes, *Thin Solid Films* **89**, 249 (1982).
- P. K. Tien, *Appl. Opt.* **10**, 2395 (1971).
- K. K. Lee, D. R. Lim, H. C. Luan, A. Agarwal, J. Foresi, and L. C. Kimerling, *Appl. Phys. Lett.* **77**, 1617 (2000).
- G. Lerondel, R. Romestain, and S. Barret, *J. Appl. Phys.* **81**, 6171 (1997).
- K. K. Lee, D. R. Lim, L. C. Kimerling, J. Shin, and F. Cerrina, *Opt. Lett.* **26**, 1888 (2001).
- BeamPROP by RSoft, www.rsoftdesign.com.
- D. Marcuse, *Bell Syst. Tech. J.* **48**, 3187 (1969).