

Growth of high quality Er–Ge films on Ge(001) substrates by suppressing oxygen contamination during germanidation annealing

S.L. Liew^a, B. Balakrisnan^a, S.Y. Chow^a, M.Y. Lai^a, W.D. Wang^a, K.Y. Lee^a,
C.S. Ho^b, T. Osipowicz^c, D.Z. Chi^{a,*}

^a Institute of Materials Research and Engineering, 3 Research Link, Singapore 117602, Singapore

^b Department of Mechanical and Production Engineering, Faculty of Engineering, National University of Singapore, 10 Kent Ridge Crescent, Singapore 119260, Singapore

^c Department of Physics, Lower Kent Ridge Road, National University of Singapore, Singapore 117542, Singapore

Available online 7 October 2005

Abstract

Solid-state reactions between Er and Ge (001) under different processing conditions were investigated. Under normal rapid thermal processing (RTP) in high-purity N₂ ambience, the Er–Ge film formation was ‘contaminated’ with Er₂O₃ even at low temperature annealing. Ti capping of Er films before RTP delayed Er₂O₃ formation with the Ti cap acting as a sacrificial layer for the Er underneath. Vacuum annealing of Er films significantly reduced Er₂O₃ formation even after higher temperature annealing. High quality Er–Ge films can thus be formed through solid-state reaction of Er and Ge if oxygen contamination from annealing ambient during RTP is controlled. The Er–Ge phase had low sheet resistance values averaging 3 to 4 Ω/sq. ErGe_{1.8} was formed from the solid-state reaction between Er and Ge(001) in vacuum.

© 2005 Elsevier B.V. All rights reserved.

Keywords: Rapid thermal processing; Erbium; Germanium

1. Introduction

The solid-state reactions between rare earth metals and germanium/silicon have interested researchers for both fundamental investigations as well as for their relevance to functional device fabrication [1–3]. The microelectronics industry is actively evaluating Ge as a promising alternative to Si as some fundamental limitations related to the aggressive scaling (or miniaturization) of metal-oxide-semiconductor field effect transistors (MOSFETs) can be overcome by using higher carrier mobility substrate materials such as Ge [4]. While the use of higher carrier mobility substrates (strained Si and SiGe currently and Ge in future) is the current industrial trend, further improvement of device performance requires the use of new device architectures such as Schottky barrier source/drain (SSD) MOSFETs in order to maintain the source and drain resistance to a reasonable fraction (~10%) of the channel resistance. It is believed that for Ge-based MOSFETs, the most

likely candidate materials for this application are some metallic germanides with the right work functions since the highest quality interface can be ensued in the Schottky barriers formed by the solid-state reaction between metals and Ge. Earlier work on SiGe suggests that PtSi(Ge)/PtGe might be suitable candidates to form SSD in Si(Ge)- and Ge-based PMOS transistors [5]. However for NMOS transistors, there has been no serious attempt to identify suitable germanosilicide/germanide materials for the same application although ErSi₂ and DySi₂ have been shown to yield low Schottky barrier heights on n-Si [6]. In this context, it is important to study the formation of Er–Ge phases as SSD for Ge-based NMOS transistors. However rare-earth metals are reactive with oxygen and different processing conditions are expected to have significant influence on the germanide formation. In this study, we have elucidated the solid-state reactions between Er and Ge (100) under different processing conditions.

2. Experimental procedures

Ge(001) wafers (n type, 0.4 Ω cm) were dipped in diluted HF solution to remove native oxides from the surfaces. After

* Corresponding author. Tel.: +65 6874 8356; fax: +65 6872 0785.

E-mail address: dz-chi@imre.a-star.edu.sg (D.Z. Chi).

loading the wafers into the deposition chamber of a d.c. magnetron sputtering system, the chamber was pumped down to a base pressure of at least 5×10^{-7} Torr with a minimum pumping down time of <10 min. 35 nm thick Er was sputter-deposited onto the wafers while 15 nm thick Ti was deposited onto the Er layer for some samples (labelled as capped samples) without breaking the vacuum. Annealing of the samples was carried out in a rapid thermal annealing (RTA) chamber. Er/Ge and Ti/Er/Ge samples were annealed in either N_2 ambience or vacuum. In all the three sets of samples, RTA was carried out for 60 s at temperatures ranging from 300 to 600 °C.

Electrical and material characteristics of the samples were analysed with four-point probe method, scanning electron microscopy (SEM), X-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscopy (TEM).

3. Results and discussion

Fig. 1a shows the XRD spectra of Er/Ge(001) samples annealed in N_2 . At 400 °C, an asymmetrical peak with maxima at $2\theta \approx 30^\circ$ appeared. This value is close to the value reported in the PDF for $Er_2O_3(111)$ and Er–Ge phases [7]. It is possible that annealing at low temperature in N_2 already resulted in the formation of oxides with Er–Ge phases. This speculation is supported by the XRD patterns for Ti/Er/Ge(001) sample annealed at the same temperature (Fig. 1b) which show that $Er_2O_3(111)$ was absent from 300 to 500 °C, suggesting that the Ti layer inhibited the oxidation of Er during annealing. However at 600 °C, strong Er_2O_3 peaks appeared for both uncapped and capped samples, showing that the Ti layer was no longer effective against oxidation at higher temperature. The dominant peaks detected from the Ti-capped sample ($2\theta \approx 26.2^\circ, 34.3^\circ$) corresponded to Er–Ge phases. In contrast, a different observation was obtained with vacuum-annealed samples (Fig. 1c). Only one peak at $2\theta \approx 30^\circ$ was observed at 300 °C. As $Er_2O_3(111)$ and Er–Ge phase have very close 2θ values, it is possible that both the oxide and germanide co-existed at 300 °C. As the temperature increased, additional peaks were detected with peaks at $2\theta \approx 26.1^\circ$ and 34.2° also observed in the Ti/Er/Ge(001) samples. Compared to annealing in N_2 ambience, the Er_2O_3 formation was significantly reduced even up to high temperatures. The intensity of the Er_2O_3 peak was also constant with temperature.

Although the structures and phases in bulk Er–Ge had been investigated previously [8–10], the identification and evolution of Er–Ge phases in thin film formation has not been reported. RBS employing 2 MeV He^+ to profile the elemental ratio of Er to Ge with depth was carried out. Fig. 2 shows the RBS spectra of Er/Ge(001) annealed at 300 and 600 °C in vacuum. At 300 °C, the edge of the Er signal is relatively straight, suggesting a smooth interface between the Er–Ge layer and Ge. This was shown in the TEM image. It was found that the Er–Ge layer also consisted of amorphous phase.

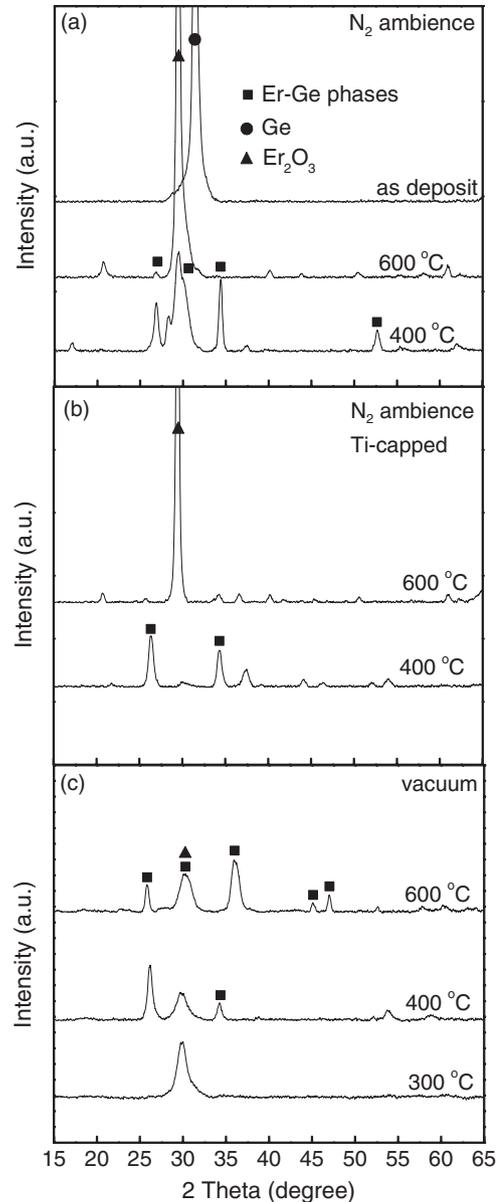


Fig. 1. XRD spectra of Er/Ge(001) samples obtained under different processing conditions. (a) Annealed in N_2 ambience. (b) Ti-capped samples annealed in N_2 ambience. (c) Annealed in vacuum.

Amorphous interlayer had been reported to form first between rare-earth metals and Si substrate upon annealing [11,12]. The amorphous Er–Ge formation also indicated that the XRD peak reported earlier is due to Er_2O_3 formation. The left-hand side of the Er signal displayed a significant slope when the temperature increased to 600 °C and this coincided with an uneven interface between the Er–Ge layer and Ge. The RBS experimental data were fitted with RUMP program. The stoichiometric ratios of Ge/Er were 1.2 and 1.8 for 300 and 600 °C, respectively. The phase $ErGe_{1.8}$ agreed with that reported for $YGe_{1.7}$ and $TbGe_{1.7}$ since these three rare-earth metals (Er, Y and Tb) have close-packed hexagonal structures with close lattice parameters [1].

Depth-profiling of Er/Ge(001) samples annealed under different conditions at 400 °C was obtained by SIMS. Fig. 3a

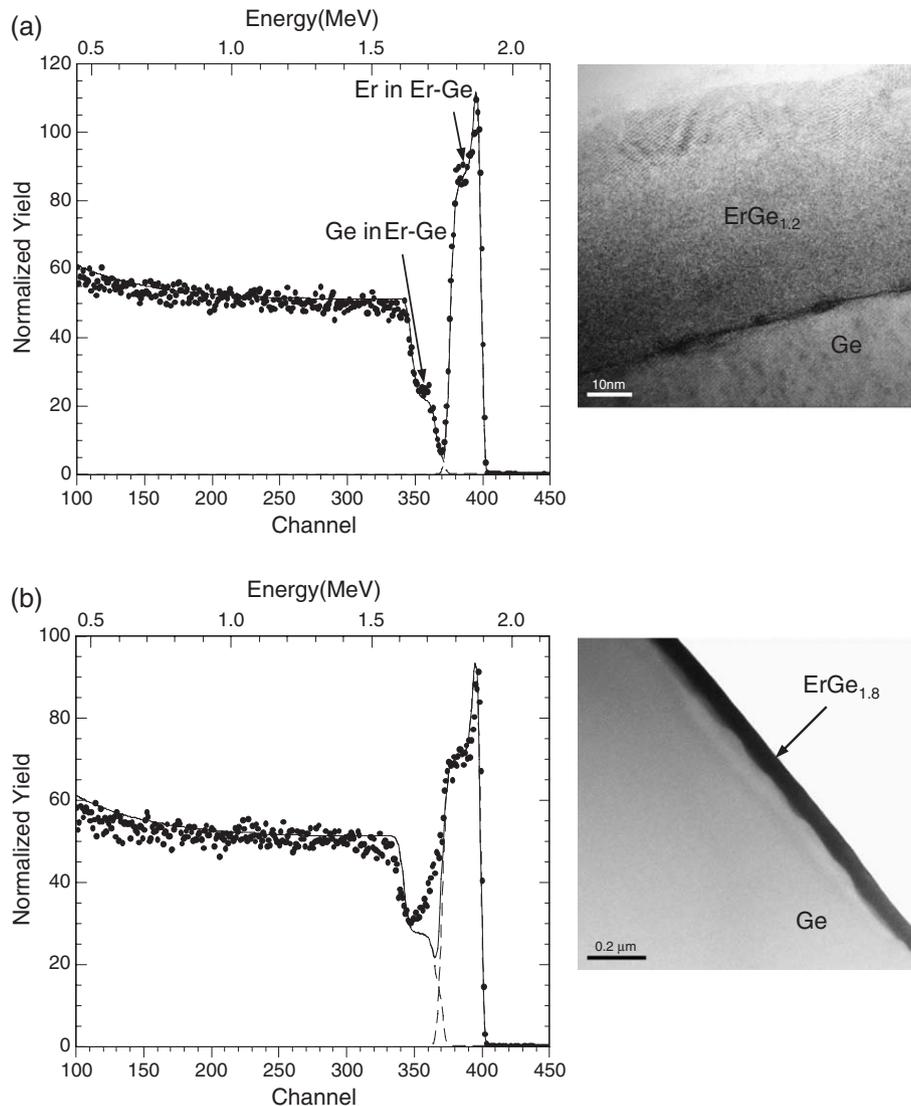


Fig. 2. RBS spectra and TEM images of Er/Ge(001) annealed in vacuum, (a) 300 °C, (b) 600 °C.

shows a relatively thick Er_2O_3 layer was formed upon N_2 annealing which confirmed the presence of the strong oxide peak in the XRD scan in Fig. 1a. With a Ti capping layer or vacuum annealing, the Er_2O_3 formation was reduced (Fig. 3b and c) which is consistent with the lower intensities observed in the XRD patterns (Fig. 1).

The thickened oxide layer resulting from N_2 annealing created crack-like features on the surface morphology at higher temperature, as shown in Fig. 4. These cracks, averaging 1 μm in size, appeared to protrude from the surface and it is possible that their depths were contained within the oxide layer. It is likely that the cracks were formed to relieve stress in the thick Er_2O_3 layer. On the other hand, films capped with Ti and those annealed in vacuum had smooth morphology without the crack-like features. The oxide layers were significantly reduced (see SIMS plots in Fig. 3) in these cases such that crack formation was avoided. Defects such as pits and pinholes had been reported to form in Er silicide thin films even when they were annealed in vacuum conditions [2]. It is possible that the annealing was done at higher

temperature or with extended times in these studies whereas RTA was used to anneal our samples such that no defects were formed in the films.

The Er–Ge phase formation can be correlated to the plot of sheet resistance values in Fig. 5. Er/Ge(001) annealed in N_2 had higher sheet resistance values than those annealed in oxygen-controlled ambience. Vacuum-annealed and Ti-capped samples had minimum sheet resistance values of 3 to 4 Ω/sq , showing that Er–Ge film can be used as a low resistivity metallization contact. However the temperature range for minimum sheet resistance for both Ti-capped and vacuum-annealed samples is only from 400 to 500 °C. For the vacuum-annealed samples, the high sheet resistance at 300 and 600 °C is probably due to thinner germanide layer formed and uneven interface between $\text{ErGe}_{1.8}$ and Ge, respectively (see Fig. 2). There is no known data available on the electrical resistivities of Er–Ge phases however. The sheet resistance of Ti-capped samples had the same profile as the vacuum-annealed samples. The higher value at 300 °C can be explained by the formation of titanium oxide (see SIMS plot in Fig. 3b) while that at 600

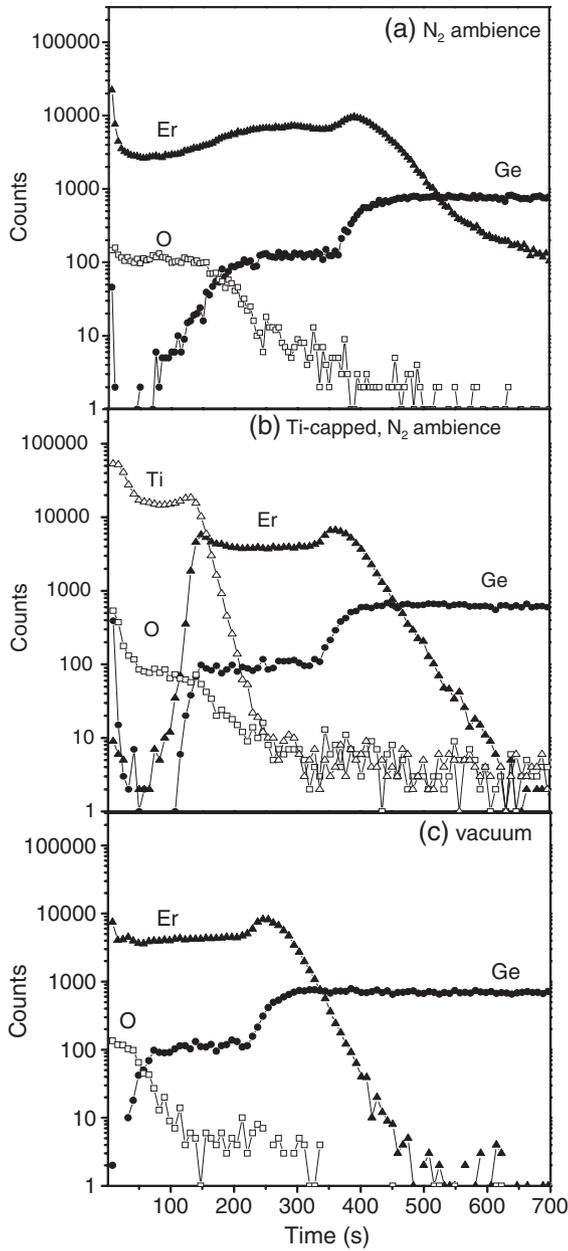


Fig. 3. SIMS plots of Er/Ge(001) annealed at 400 °C under different processing conditions. (a) Annealed in N₂ ambience. (b) Ti-capped samples annealed in N₂ ambience. (c) Annealed in vacuum.

°C is due to Er₂O₃ formation which escalated the sheet resistance (see XRD diagrams in Fig. 1). Ti could have diffused into the underlying Er to get oxygen incorporated in the Er film during sputtering which left the Er layer unprotected against oxidation.

In conclusion, the formation of Er–Ge films under different processing conditions was studied. Annealing in oxygen-controlled ambience is needed to achieve high quality Er–Ge films without Er₂O₃ contamination. Ti capping and vacuum annealing of Er films delayed and significantly reduced Er₂O₃ formation, respectively, resulting in defect-free film morphologies. The Er–Ge phase had low sheet resistance values averaging from 3 to 4 Ω/sq. ErGe_{1.8} was formed from the solid-state reaction between Er and Ge(001) in vacuum.

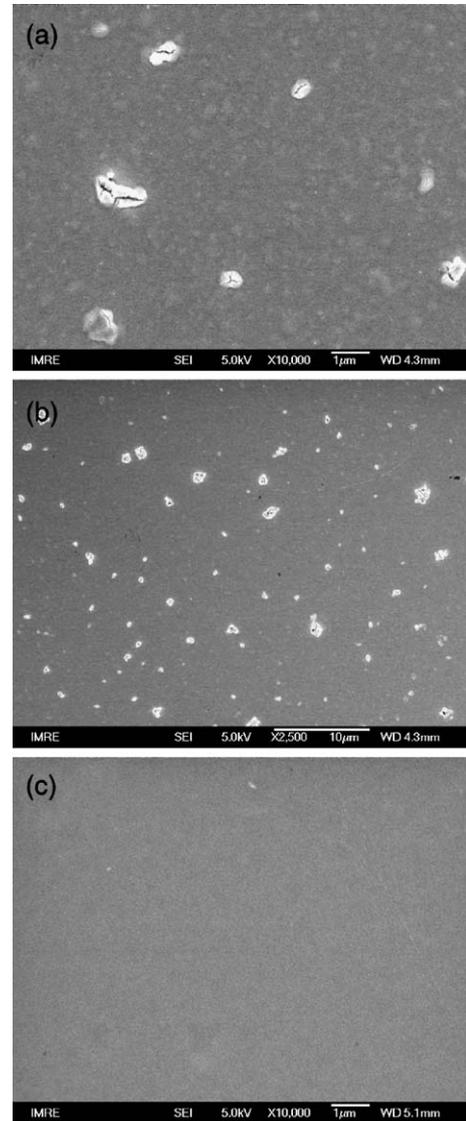


Fig. 4. Surface morphology of Er/Ge(001) annealed at 500 °C. (a) Annealed in N₂ ambience. (b) Lower magnification, showing the distribution of crack-like features. (c) Annealed in vacuum.

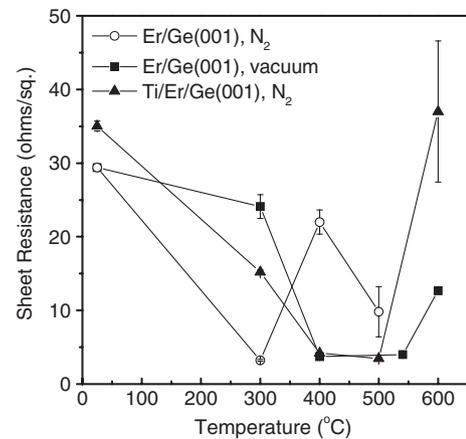


Fig. 5. Sheet resistance values of Er/Ge(001) samples obtained under different processing conditions.

References

- [1] J.E.E. Baglin, F.M. d'Heurie, C.S. Petersson, *J. Appl. Phys.* 52 (1981) 2841.
- [2] S.S. Lau, C.S. Pai, C.S. Wu, T.F. Kuech, B.X. Liu, *Appl. Phys. Lett.* 41 (1982) 77.
- [3] W.C. Tsai, K.S. Chi, L.J. Chen, *J. Appl. Phys.* 96 (2004) 5353.
- [4] C.O. Chui, H. Kim, D. Chi, B.B. Triplett, P.C. McIntyre, K.C. Saraswat, *IEEE Electron Devices Meet.* (2002) 437.
- [5] T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, S. Takagi, *IEEE Electron Device Lett.* 26 (2005) 102.
- [6] S. Zhu, J. Chen, M.F. Li, S.J. Lee, J. Singh, C.X. Zhu, A. Du, C.H. Tung, A. Chin, D.L. Kwong, *IEEE Electron Device Lett.* 25 (2004) 565.
- [7] Erbium Oxide Powder Diffraction File No. 8-50, Erbium Germanium Joint Committee on Powder Diffraction Standards (JCPDS) No. 85-2338.
- [8] O.Ya. Oleksyn, O.I. Bodak, *J. Alloys Compd.* 210 (1994) 19.
- [9] P. Schobinger-Papamantellos, G. André, J. Rodríguez-Carvajal, C.H. de Groot, K.H.J. Buschow, *J. Alloys Compd.* 232 (1996) 165.
- [10] O. Oleksyn, P. Schobinger-Papamantellos, C. Ritter, C.H. de Groot, K.H.J. Buschow, *J. Alloys Compd.* 252 (1997) 53.
- [11] T.L. Lee, L.J. Chen, *J. Appl. Phys.* 73 (1993) 5280.
- [12] C.H. Luo, L.J. Chen, *J. Appl. Phys.* 82 (1997) 3808.